PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD/13/7867
Dated 23 May 2013

Conversion to ECOPACK 2 in the ISOTOP packages manufactured in the ST's plant of Boskoura Morocco

Table 1. Change Implementation Schedule

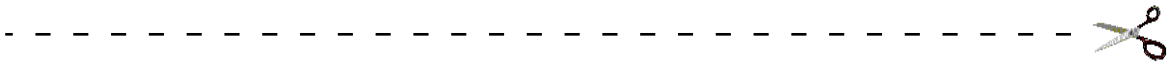
Forecasted implementation date for change	19-Aug-2013
Forecasted availability date of samples for customer	23-May-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	16-May-2013
Estimated date of changed product first shipment	22-Aug-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	To implement ECOPACK 2
Description of the change	To move from standard to massive production of ECOPACK 2 graded supply and complete the move to DBC assembly technology. The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets. An exception regarding thermal performance, will affect the following four part numbers: STTH20004TV1, STTH200L04TV1, STTH200R04TV1 and STTH200F04TV1. Please refer to the latest datasheets version published on ST.com, to review updated data. There is as well no change in the packing process nor in the standard delivery quantities.
Change Product Identification	by the removal of the 2LI (2nd Level Interconnect) logo
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD/13/7867**
Please sign and return to STMicroelectronics Sales Office	**Dated 23 May 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

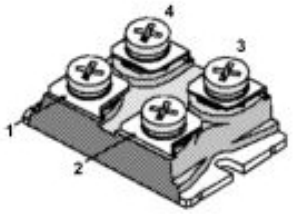
Name	Function
Giuffrida, Antonino	Marketing Manager
Martelli, Nunzio	Product Manager
Vitali, Gian Luigi	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

IPD Group

Conversion to ECOPACK®2 (also called Halogen_Free) for products housed in the ISOTOP packages manufactured in the ST's plant of Boskoura Morocco.

Packages typology



ISOTOP

Premise

The ECOPACK® program is the cornerstone of our effort of being a leader in the change toward environmentally friendly packaging. In the context of this program, ST develops world class technical solutions designed to progressively remove banned substances from manufacturing.

Continuing in the already announced plan of moving the supply to the ECOPACK®2 grade products (also known in the market as "Halogen Free") and in the aim of a constant process improvement, Isotop package will be from now available as ECOPACK®2 graded.

WHY THIS CHANGE?

To implement ECOPACK®2 grade supply for: PowerBipolar, IGBT, PowerMOSFET and Rectifiers products housed in the ISOTOP package.

This PCN is intended as well for announcing the move from aluminium ceramic (ALN/AL2O3) to the use of DBC ceramic (Direct bonding copper) for the Rectifiers products .

WHAT IS THE CHANGE?

To move from standard to massive production of ECOPACK®2 graded supply and complete the move to DBC assembly technology.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets. An exception regarding thermal performance, will affect the following four part numbers: STTH20004TV1, STTH200L04TV1, STTH200R04TV1 and STTH200F04TV1. Please refer to the latest datasheets version published on ST.com, to review updated data.

There is as well no change in the packing process nor in the standard delivery quantities.

WHEN?

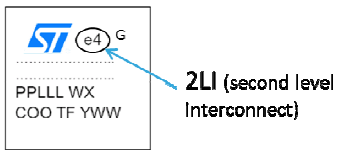
For the products listed in the attached document, the availability will be granted according the following schedule:

Product Family	Package/s	Samples	Full Production
Power Bipolar&IGBT	ISOTOP	Wk 20 (*) '13	Wk 34 '13
PowerMOSFET	ISOTOP	Wk 20 (*) '13	Wk 34 '13
Rectifiers	ISOTOP	Wk 20 (*) '13	Wk 34 '13

(*) For Test Vehicle – For other samples please contact local Sales Organization

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set, will be easily identified thanks to the traceability code indicated on the inner and external label and visible by the removal of the 2LI (2nd Level Interconnect) logo (e4) from top of the package, since no more required.



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Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.

After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

Qualification Data:

First qualification report will be available upon request starting wk 20_ 2013

Please note that ST Team is doing all the best for providing you full visibility about these announced changes and to minimize any negative impact it may occur.
While our Marketing and Sales teams are available for additional information when required, we are looking forward to your renewed confidence in STMicroelectronics as the strategic partner of your choice.

Qualification of
Rectifier products in ISOTOP package: Conversion to ECOPACK®2 grade with structure rationalization

General Information	
Product Line	Rectifiers
Product Description	Rectifiers in ISOTOP package: ECOPACK®2 resin and DBC ceramic
Product Group	IPD
Product division	ASD & IPAD
Package	ISOTOP
Maturity level step	Qualified

Locations	
Wafer fab	STM France STM Singapore
Assembly plant	STM Bouskoura (Morocco)
Reliability Lab	STM Tours (France)

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	22-Feb-2013	8	I. BALLON	First issue Qualification of Rectifier products in ISOTOP package: Conversion to ECOPACK®2 grade with structure rationalization

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
FMEA	8423373
RER	1226004

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
uHAST	Unbiased Highly Accelerated Stress Test
THB	Temperature Humidity Bias
IOLT	Intermittent Operational Life
RSH	Resistance to Solder Heat
	Screwing

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify ECOPACK®2 (“Halogen-Free”) encapsulation molding compound and standardization to DBC ceramic (Direct Bonding Copper) for all Rectifiers housed in ISOTOP package manufactured in ST Bouskoura plant (in Morocco).

The involved product series are listed in the table below:

Package	ECOPACK®2 conversion	Involved Product Series
ISOTOP	**All**	STTHxxxxTV/TV1/TV2 STPSxxxxTV/TV1/TV2

The reliability methodology used in this qualification follows the JESD47-G: «Stress Test Driven Qualification Methodology».

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

- Rectifiers housed in ISOTOP package manufactured in ST Bouskoura plant (Morocco): ECOPACK®2 (“Halogen-Free”) encapsulation molding compound and DBC ceramic.

4.2 Construction note

	Rectifiers in ISOTOP package
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore ST Tours (France)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore ST Tours (France)
Assembly information	
Assembly site	ST Bouskoura (Morocco)
Package description	ISOTOP
Molding compound	**ECOPACK®2** (“Halogen-free”) molding compound
Frame material	Copper
Die attach process	Soft solder
Die attach material	Preform Pb/Sn/Ag
Wire bonding process	Ultra Sonic wire bonding
Wires bonding materials	Aluminium
Lead finishing material	Nickel
Final testing information	
Testing location	ST Bouskoura (Morocco)

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Process/ Package	Product Family	Product
1	ISOTOP	Power Schottky	STPS200170TV1Y
2		Turboswitch	STTH12012TV1
3		Bipolar	STTH16003TV1
4		Power Schottky	STPS80H100TV

5.2 Test plan and results summary

Die Oriented Tests

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		Note
						Lot 1	Lot 4	
HTRB	N	JESD22 A-108	Tj, Vr = 0.8xVrrm	154	168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	

Package Oriented Tests

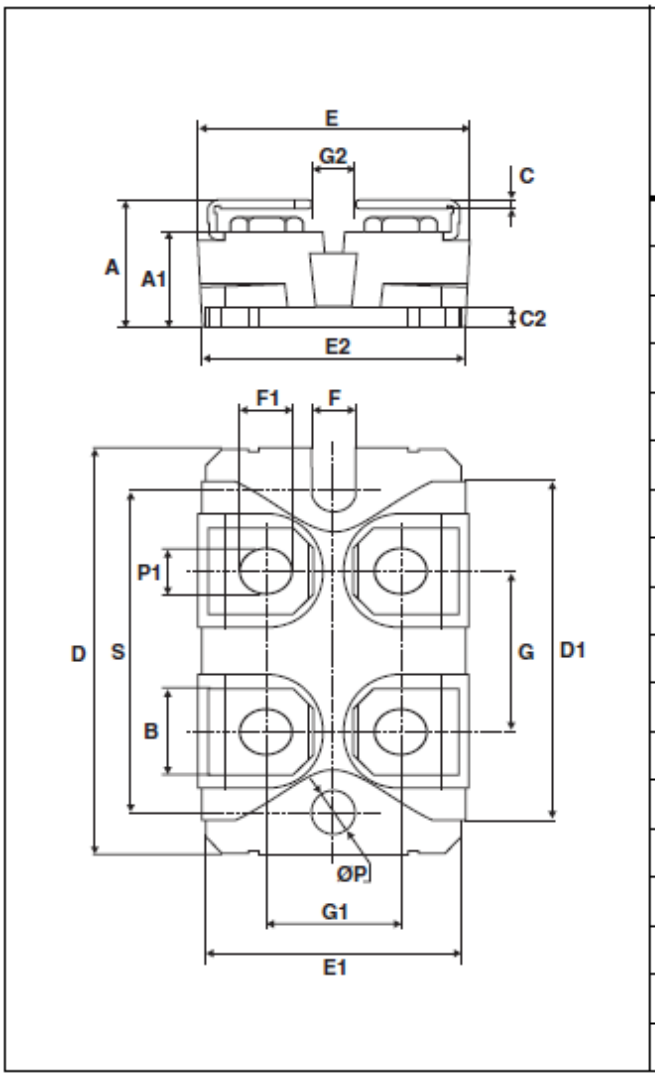
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2		
THB	N	JESD22 A-101	Ta = 85°C, RH = 85%, Vr = 0.8xVrrm or 100V max	154	168 H	0/77	0/77		
					500 H	0/77	0/77		
					1000 H	0/77	0/77		
				SS	Steps	Failure/SS			Note
						Lot 1	Lot 2		
TC	N	JESD22 A-104	Ta = -65°C to 150°C 2 cycles/hour	102	500 cy	0/77	0/25		
					1K cy	0/77	0/25		
				SS	Steps	Failure/SS			Note
						Lot 1			
IOLT	N	MIL-STD 750 Method 1037	Delta Tc=85°C, Pon=5min Poff=5min	77	3k cy	0/77			
					6k cy	0/77			
				SS	Steps	Failure/SS			Note
						Lot 1			
RSH	N	JESD22B-106	2 dipping at 260°C 10s On / 15s Off	12	Final test	0/12			
				SS	Steps	Failure/SS			Note
						Lot 1			
uHAST	N	JESD22 A118	Ta=130°C, RH=85%, P=3bars	77	96hrs	0/77			
				SS	Steps	Failure/SS			Note
						Lot 3			
Screwing	N	ST 0063378	1.5N.m	7	Final test	0/7			

6 ANNEXES

6.1 Device details

6.1.1 Package outline/Mechanical data

- **ISOTOP**



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	11.80	12.20	0.465	0.480
A1	8.90	9.10	0.350	0.358
B	7.8	8.20	0.307	0.323
C	0.75	0.85	0.030	0.033
C2	1.95	2.05	0.077	0.081
D	37.80	38.20	1.488	1.504
D1	31.50	31.70	1.240	1.248
E	25.15	25.50	0.990	1.004
E1	23.85	24.15	0.939	0.951
E2	24.80 typ.		0.976 typ.	
G	14.90	15.10	0.587	0.594
G1	12.60	12.80	0.496	0.504
G2	3.50	4.30	0.138	0.169
F	4.10	4.30	0.161	0.169
F1	4.60	5.00	0.181	0.197
P	4.00	4.30	0.157	0.69
P1	4.00	4.40	0.157	0.173
S	30.10	30.30	1.185	1.193

6.2 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
uHAST	The device is placed under 130°C 85% RH during 96 hours.	The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test (THB).

Test name	Description	Purpose
IOLT	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors), followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
RSH	The device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

Reliability Report

ISOTOP ECOPACK® 2 graded molding compound qualification – ST BOUSKOURA Assy plant (Morocco)

General Information	
Product Lines:	MD6N
Product Families:	Power MOSFET
P/Ns:	STE70NM60
Product Group:	IMS - IPD
Product division:	Power Transistor Division
Package:	ISOTOP
Silicon Process techn.:	StripFET™- MDMesh™

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (SINGAPORE)*
EWS Plants:	*Ang Mo Kio (SINGAPORE)*
Assembly plant:	*BOUSKOURA (Morocco)*
Reliability Lab:	*IMS-IPD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	April 2013	6	C. Cappello	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the ISOTOP package graded Molding Compound manufactured in the ST Bouskoura (Morocco) assy plant.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STE70NM60 LINE: MD6N PACKAGE: ISOTOP

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	StripFET™- MDMesh™
Die finishing back side	Ti/Ni/Ag
Die size	9610 x 12640 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	Bouskoura (Morocco)
Package description	ISOTOP
Molding compound	HF Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 7 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Bouskoura (Morocco)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1-2	STE70NM60	MD6N	Power MOSFET

5.2 Reliability test plan summary

Lot. 1-2 - D.U.T.: STE70NM60 LINE: MD6N PACKAGE: ISOTOP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	
						Lot 1	Lot 2
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	154	168 H 500 H 1000 H	0/77	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	154	168 H 500 H 1000 H	0/77	0/77
HTSL	N	JESD22 A-103	TA = 150°C	154	168 H 500 H 1000 H	0/77	0/77
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	154	168 H 500 H 1000 H	0/77	0/77
TC	N	JESD22 A-104	TA=-40°C TO 150°C (1 HOUR/CYCLE)	154	100 cy 200 cy 500 cy 1000 cy	0/77	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	154	96 H	0/77	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.